Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 70011

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2025
Third Semester
Power Systems Engineering
P23VDOE2 – BASICS OF VLSI
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Define Moore's law.	2	K2	CO1
2.	Write a short note on VLSI design flow.	2	K2	CO1
3.	Define twin tub process.	2	K1	CO2
4.	List the CMOS fabrication processes.	2	K2	CO2
5.	Recall Domino and Pass transistor logic.	2	K2	CO3
6.	Define body effect.	2	K1	CO3
7.	Compare PAL and PLA.	2	K2	CO4
8.	Write a short note on CPLD.	2	K1	CO4
9.	Show the truth table of AND gate primitive.	2	K2	CO5
10.	List the four levels in Verilog HDL.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Discuss in detail about the following MOSFET types: i. Enhancement P-Type MOSFET ii. Depletion P-Type MOSFET	13	K2	CO1
		(OR)			
	b)	Summarize the stick diagrams of NMOS and CMOS encoding and also comments on the rules to be followed.	13	K2	CO1
12.	a)	Discuss in detail about the fabrication process steps of nMOS transistor with necessary diagrams.	13	K2	CO2
		(OR)			
	b)	Discuss in detail about the twin tub CMOS fabrication process with necessary diagrams.	13	K2	CO2
13.	a)	With necessary diagrams, discuss about pseudo nMOS DC operation and also mention its advantages and disadvantages.	13	K2	CO3
		(OR)			
	b)	With necessary diagrams, discuss in detail about CVSL and also comment on its application.	13	K2	CO3
14.	a)	Explain the logic diagram of the CPLD with a suitable diagram.	13	K2	CO4
		(OR)			
	b)	Discuss in detail about the issues in FPGA and also comment on altera FPGA.	13	K2	CO4
15.	a)	Discuss in detail about Tri-state gate with a suitable diagram.	13	K2	CO5
		(OR)			
	b)	Explain combinational and sequential UDPs with a suitable example.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Analyze the function of two input NOR and NAND gate with its layout and stick diagram.	15	K2	CO1
		(OR)			
	b)	Analyze the ionization structures of Silicon on Insulator (SOI) Bipolar and CMOS on same chip (BiCMOS) and also comment on LOCOS.	15	K3	CO3